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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,089	08/01/2003	Olav Tirkkonen	59643-00238	3395

32294 7590 12/08/2006

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EXAMINER	
NGUYEN, DUC M	

ART UNIT	PAPER NUMBER
2618	

DATE MAILED: 12/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	Application No. 10/632,089	Applicant(s) TIRKKONEN ET AL.	
	Examiner Duc M. Nguyen	Art Unit 2618	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 20 November 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires *4* months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1-23*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See the attached "Response to Arguments".
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

Response to Arguments

1. Applicant's arguments filed 11/20/06 have been fully considered but they are not persuasive.

As to claims 1, 18, 23, regarding a power allocation algorithm and bit loading sequence, Applicant contends that

" Sadjadpour does not teach or suggest circuitry configured to select a bit loading sequence with a lowest error rate, as recited in claim 1. Similarly, Sadjadpour also does not teach or disclose a selecting means for selecting a bit loading sequence with a lowest error rate, as recited in claim 23. Further, Sadjadpour does not teach or disclose determining a power allocation for at least one bit loading sequence based on minimizing an error rate, as recited in claim 18.

More particularly, with regard to claims 1 and 23, the Examiner has indicated that Sadjadpour discloses the circuitry recited in claims 1 and 23 in paragraphs [0043]-[0046]. These paragraphs of Sadjadpour, which describe Figure 6, show the various inputs which are required in order to operate the bit allocation algorithm. Thus, blocks 61-68 represent the various objective functions with the shaded blocks of Figure 6 being those used to reduce the cross talk. Therefore, function 64 represents the joint minimization of an arbitrary function of the total power and maximization of the total data rate such as would be achieved using the algorithm described in paragraphs [0036]-[0038]. Similarly, function block 61 shows the functions which apply joint minimization of the cross talk and maximization of the total data rate, as is shown in the method described in paragraphs [0039]-[0042].

Therefore although Sadjadpour does disclose selection of a specific constellation of symbols or bits creating symbols for each sub-frequency bin dependent on minimizing power and minimizing cross talk, there is no disclosure of circuitry for selecting a bit loading sequence with the lowest error rate. As such, Applicants submit that Sadjadpour fails to teach or disclose each and every element recited in claims 1 and 23, and therefore, reconsideration and withdrawal of the rejection of claims 1 and 23 over Sadjadpour is respectfully requested".

In response, the Examiner asserts that although Sadjadpour's teaching is directed to a cross-talk reduction, Sadjadpour does teach a methodology for determining a power allocation for at least one bit loading sequence based on minimizing an error rate, as recited in each of claims 1, 18, and 23.

In fact, since Sadjadpour does teach a bit and power allocation algorithm for a selected function to be optimized (see Fig. 6 and [0045], [0046]), and since the selected function to be optimized comprises a function 62 that minimizes the bit-error-rate BER (see [0044]), it is clear that Sadjadpour would teach, or implicitly teach, a bit loading and power allocation algorithm for minimizing BER. By minimizing BER, it is clear that the lowest BER is selected. Here, although function 62 provides a joint minimization of the BER and maximization of the total data rate, the BER minimization criteria would read on the claimed limitation

"circuitry for determining a power allocation for at least one bit loading sequence based on minimizing an error rate; and

circuitry for selecting a bit loading sequence with a lowest error rate".

Also note that since Sadjadpour does teach that the bit allocation algorithm and power allocation needed are re-calculated and re-sorted (see [0038]), it is clear that there is variability of the power allocation of the selected bit loading in order to minimize an error rate, as recited in Applicants' claims.

Further, although the Examiner has specifically pointed out the function 62 in the previous response (Final Office Action) regarding the BER minimization, this function is not mentioned by Applicant in the argument, instead, only functions 61 and 64 are

specifically mentioned by Applicant. Accordingly, Examiner assumes that Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

As to claims 19-20, 22, the same argument/response regarding the power allocation and selecting a bit loading sequence with a lowest error rate features as mentioned above can also be applied here.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, since the use of a MIMO system for improving performance (i.e, increase transmission capacity) of a communication device is well known in the art, one skilled in the art would recognize the benefit (i.e, maximum throughput) of the MIMO system in Applicant's admitted prior art (AAPA) to incorporate Sadjadpour's teaching to the MIMO system in AAPA as well, for providing a MIMO system as claimed, for improving the performance a communication device.

For foregoing reasons, the examiner believes that the pending claims 1-23 which rely on the patentability of a power allocation feature and a bit loading sequence based on the lowest BER are not allowable over the cited prior art.

2. **Any response to this action should be mailed to:**

Box A.F.

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(571) 273-8300 (for **formal** communications intended for entry)

(571)-273-7893 (for informal or **draft** communications).

Hand-delivered responses should be brought to Customer Service Window, Randolph Building, 401 Dulany Street, Alexandria, VA 22314.

Any inquiry concerning this communication or communications from the examiner should be directed to Duc M. Nguyen whose telephone number is (571) 272-7893, Monday-Thursday (9:00 AM - 5:00 PM).

Or to Matthew Anderson (Supervisor) whose telephone number is (571) 272-4177.

Duc M. Nguyen, Primary Examiner

Dec 4, 2006